A Novel Digital Hysteresis Current Controller for an Active Power Filter

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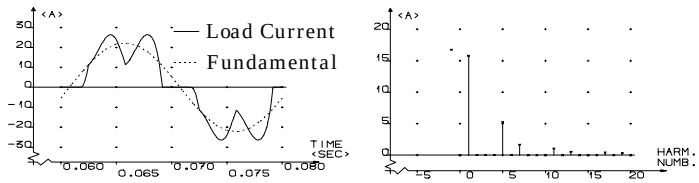
Abstract An active power filter is used to eliminate current harmonics produced by non-linear loads. This paper discusses a novel method of controlling a power inverter used to inject compensating currents into the power system. A digital signal processor performs the harmonic isolation and generates a digital reference current. A hysteresis current controller has been implemented in a field programmable gate array and generates the switching signals from this reference. This reduces the analogue circuitry and enhances the system's immunity to noise. This paper presents the results and discusses the performance of a small scale inverter under completely digital control.

1. Introduction

1.1 The Active Power Filter

Current harmonics produced by non-linear loads (such as switching power supplies and motor speed controllers) are prevalent in today's power systems. These harmonics interfere with sensitive electronic equipment and cause unnecessary losses in electrical machinery. Shunt active filters were initially proposed in 1971 by Sasaki and Machida [1] as a means of removing current harmonics. It is only with the recent advances in semiconductor technology that high-speed, high-power devices suitable for constructing active power filters have come available [2].

Typical three-phase rectifier supply currents (I_L in Figure 2) are shown in Figure 1. The fundamental component of the supply current is shown, since this is the waveform that the power system will supply after compensation (I_S in Figure 2).



(a) (b)

Figure 1 Load current for a three-phase bridge rectifier in (a) the time domain and (b) the frequency domain.

Figure 2 shows a single phase system diagram for the active power filter. The three phase inverter injects compensating currents into the power system. A capacitor is used for energy storage, is charged by the power system and maintained at a constant DC voltage. The only real power used is due to losses in the inverter. Once the load current, I_L, is fully compensated by the active power filter the supply current, I_S, will be sinusoidal.

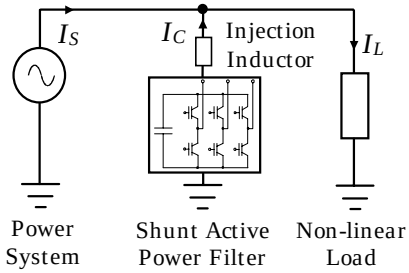


Figure 2 System diagram of an active power filter.

1.2 Elements of the Active Power Filter

There are two major parts of an active power filter. The first is the controller that determines the harmonics that are to be eliminated and maintains a stable DC bus voltage. The active power filter controller is implemented with a digital signal processor (DSP) and has been used in previous active power filtering work [3]. Several algorithms will be implemented and evaluated using this controller. This however, is beyond the scope of this paper and will be presented in a future publication.

Secondly, a three-phase inverter is used to inject the compensating currents (I_C in Figure 2) into the power system. A small scale test inverter has been built using insulated gate bipolar transistors (IGBT). There are a variety of methods for implementing each of these parts. This paper focuses on a novel method of controlling the three phase inverter.

1.3 Hysteresis Current Control

Hysteresis current control is a method of controlling a voltage source inverter so that an output current is generated which follows a reference current waveform. This method controls the switches in an inverter asynchronously to ramp the current through an inductor up and down so that it follows a reference. Hysteresis current control is the easiest control method to implement [4]. One disadvantage is that there is no limit to the switching frequency, but additional circuitry can be used to limit the maximum switching frequency. The current ramping up and down between two limits is illustrated in Figure 3.

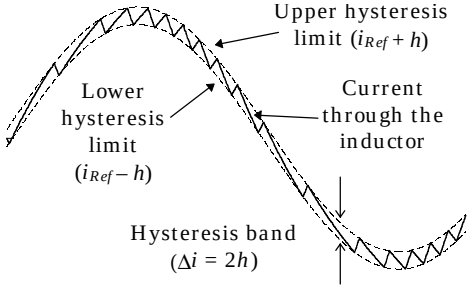


Figure 3 Hysteresis current control waveforms.

When the current through the inductor exceeds the upper hysteresis limit a negative voltage is applied by the inverter to the inductor. This causes the current in the inductor to decrease. Once the current reaches the lower hysteresis limit a positive voltage is applied, the current increases and the cycle repeats.

The switching frequency can be altered by the width of the hysteresis band, the size of the inductor that the current flows through and the DC voltage applied to the inductor by the inverter. A larger inductance has a smaller *di*/*dt* for a given voltage and so the slope of the sawtooth in Figure 3 will be shallower. Hysteresis current control leads to asynchronous switching which produces a band of switching frequencies [2].

1.4 Digital Inverter Control

The active power filter controller is implemented in a DSP. All decisions are made digitally and the current reference at any instant is represented as an integer value inside the DSP. The power switches in an inverter can either be on or off, and thus can be considered digitally. The digital inverter controller is between the DSP and inverter and uses digital communications rather than analogue signal levels. A field programmable gate array (FPGA) is the ideal means of implementing a large amount of logic in a very small space with a large degree of flexibility.

Laying an analogue circuit out on a printed circuit board takes a considerable amount of time and uses a large number of components, many of which require manual trimming. Any changes to the design would result in the procedure being repeated. A field programmable gate array is reprogrammable and this allows modifications to the inverter controller to be made internally without any changes to the printed circuit board. A consequence of using an FPGA is that the implementation is very compact.

Other digital inverter controllers have been built with DSP and programmable logic, usually erasable programmable logic devices (EPLD). One such example is in [5] where space voltage vector control was implemented with a TMS320C31 DSP and an EPLD. FPGAs are generally more flexible than EPLD for a given number of equivalent logic gates [6].

All communications between the DSP and the FPGA are at 5V logic levels, as are the switching signals from the FPGA to the inverter. Having all external communication operating at 5V, rather than small signal voltages, increases the immunity to interference. Figure 4 compares the relative magnitudes of signal and noise for large and small signals, in an analogue and digital representation. The 'Large Current' has a much larger magnitude than the noise level and consequently there is little interference. However, the 'Small Current' is smaller in magnitude than the noise, so the interference will be high. When these currents are represented digitally (with the sample taken at the circle) the magnitude is greater than the noise for both large and small currents. This ensures that the susceptibility to noise is the same for all currents when represented digitally.

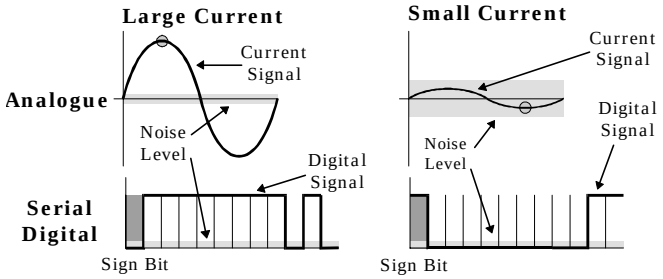


Figure 4 Comparison of analogue current signalling to digital signalling in the presence of noise.

2. Theory

2.1 Active Power Filtering Requirements

Active power filtering imposes design restrictions on the inverter that would not normally be present in other applications, for example, motor speed control. The main difference between these two applications is the maximum frequency of the current reference. An active power filter will ideally be able to compensate up to the 50th harmonic, but should at least be able to inject frequencies up to the 20th harmonic.

This high frequency operation limits the size of the injection inductor. When the inductance is too large the maximum current slope will be too shallow to track the steep current changes that occur with high frequencies. The small inductances used (typically hundreds of microhenries) mean that the rates of change of current will be high. High switching frequencies result and this causes large losses in the semiconductor switches. This also leads to increased levels of electromagnetic interference and requires very high speed comparisons of the actual current against the hysteresis limits (illustrated in Figure 3).

2.2 Injection Inductor

The injection inductor must be small enough so that the injected current *di*/*dt* is greater than that of the reference current (the compensating current signal in the active power filter) for the injected current to track the reference. Eqn. (1) gives the reference current of the highest frequency. The maximum *di*/*dt* can then be determined from Eqn. (2).

$$i(t) = A\sin(2\pi f t) \tag{1}$$

$$\max\left(\frac{di}{dt}\right) = A2\pi f \tag{2}$$

The maximum *di*/*dt* of the compensating current has to be determined for each harmonic component based on its amplitude and frequency. The overall maximum *di*/*dt* for this current is therefore the highest individual *di*/*dt*. The harmonic giving the highest *di*/*dt* is generally the third for single phase rectifiers with capacitive loads, yet is the fifth for three phase rectifiers with inductive or capacitive loads.

From the standard inductor differential equation an expression for *di*/*dt* can be determined and is given by Eqn. (3) where ΔV is the voltage across the inductor (assuming negligible resistance).

$$\frac{di}{dt} = \frac{\Delta V}{L} \tag{3}$$

The maximum inductance possible should be used in the inverter to give the lowest average switching frequency. This in turn reduces electromagnetic interference (EMI) and switching losses in the IGBTs. An expression for the maximum useable inductance is given by Eqn. (4). V_{DC} is the rail-rail DC voltage on the inverter, as illustrated in Figure 8.

$$L_{\max} = \frac{\frac{1}{2}V_{DC} - v_{\text{supply}}}{\frac{di}{dt}_{\text{Reference(max)}}} \tag{4}$$

The maximum switching frequency of a hysteresis current controlled inverter is given in [4] and reproduced in Eqn. (5). h (as illustrated in Figure 3) is the hysteresis limit and so the hysteresis band Δi is equal to $2h$.

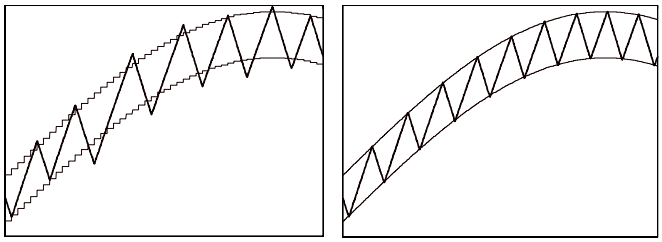
$$f_{sw(\max)} = \frac{V_{DC}}{9hL} \tag{5}$$

2.3 Sampling Frequency

Hysteresis current control requires current feedback. The sensed current is compared to the hysteresis limits and the result of this comparison is used to control the switches in the inverter.

In an analogue system the comparisons are made continuously and the current will be forced to stay within the hysteresis band at all times. With a digital controller, events happen at discrete intervals. The sensed current is digitised and the comparisons are made digitally. The current information is updated at the sampling frequency of the analogue to digital converter (ADC) that samples the current feedback. If this sampling frequency is too low there is a chance that the current will have exceeded the hysteresis limits by the time the comparison is made.

Figure 5 shows the results of a simulated inverter controller with two different sampling frequencies. It can be seen that the current regularly exceeds the hysteresis band when the current feedback is sampled too slowly.



10kHz Sampling 200kHz Sampling

Figure 5 A higher sampling frequency reduces the level of current overshoot from the hysteresis limits.

A smaller injection inductor will give a higher di/di and so the current overshoot will be greater. The worst case is where the current is just inside the hysteresis band when the comparison is made. The current will then continue on past the limit and will only reverse direction at the next sampling point. Eqn. (6) gives the maximum current overshoot Δi_{Over} for an inverter with a DC voltage V_{DC} injecting into an inductance L with a sampling frequency of f_{Sample} assuming that $v_{Supply} = 0$.

$$\Delta i_{Over} = \frac{\frac{1}{2}V_{DC}}{L}\frac{1}{f_{Sample}} \tag{6}$$

3. Inverter Controller Implementation

3.1 System Diagram

The inverter controller interfaces the digital signal processor to the three phase inverter. Figure 6 shows the inverter system with the controller, the power inverter and current feedback.

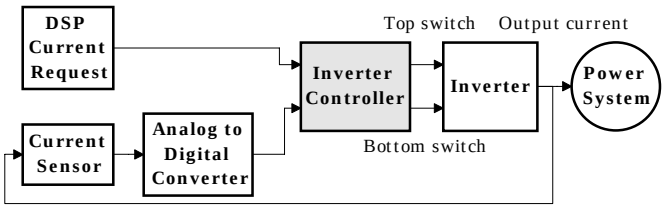


Figure 6 System diagram of the inverter and controller for one of three phases.

Figure 7 expands upon the inverter controller, highlighting the internal blocks needed for hysteresis current control. The controller is completely digital and implemented inside the FPGA.

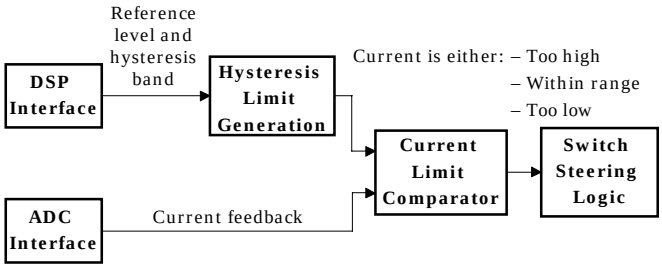


Figure 7 Block diagram of the inverter controller.

3.2 Inverter Controller Parameters

There are a few parameters to be selected for a digital hysteresis controller that are not required for an analogue controller.

Firstly, the resolution of the currents must be specified. The intended active power filter will be working with load currents up to $400A_{Peak}$ and a current precision of 0.2A is required. This gives 4000 points over the full scale of the current (from -400A to +400A). A twelve bit integer has 4096 possible values and can be used to represent the load current with the desired precision. The DSP will be working with 12 bit integers internally and will represent the compensating current as a twelve bit number. To aid the comparison of values digitally the current feedback will be digitised with a 12 bit analogue to digital converter (ADC).

Secondly, the update frequency of the reference value from the DSP and the sampling frequency of the current reference ADC must be selected. A fast sampling frequency is required for this ADC to ensure that the current ramps in the opposite direction as soon as a hysteresis limit is reached.

For a $70A_{RMS}$ compensating current a suitable value of h is 2A to 5A. Any current overshoot will add to this and should be minimal and so a suitable limit for current overshoot is 1A. The maximum inductance that can used for an active power filter injecting $60A_{RMS}$ of the 5th harmonic into a $230Vrms_{L\text{-}N}$ supply with a bus voltage of $800V_{DC}$ is 670µH. To ensure the current overshoot does not exceed 1A the sampling frequency must be at least 133kHz, as given by Eqn. (6).

A 200kHz sampling frequency has been selected for this inverter controller. This is fast enough to reduce the level of current overshoot with the inductor that will be used.

3.3 The FPGA Controller Implementation

A Xilinx XC4003A FPGA was used to implement one phase for initial testing. This FPGA is approximately equivalent to 3000 gates [6] and 85% of its resources were used.

The active power filter controller is a Texas Instruments TMS320C30 32 bit floating point DSP [7]. This communicates with the FPGA through its synchronous serial port with a 6.8MHz clock. A Maxim MAX176 12 bit serial ADC is used for the current feedback with a sampling frequency of 203kHz. This is a significant improvement over the minimum sampling requirement of 133kHz. Serial communication reduces the number of input connections to the FPGA but increases the internal logic.

Two adder/subtracters per phase generate the hysteresis limits from a reference and a hysteresis band supplied by the DSP. Two two's-complement magnitude comparators check the current feedback against these limits. Sequential logic then determines the appropriate switching pattern to drive the current in the appropriate direction through the injection inductor.

Deadtime protection is performed by a small state machine that ensures a 2µs pause between switchings. This allows for the long current tail of an IGBT and prevents 'shoot throughs' that would destroy the inverter.

4. Experimental Results

4.1 Small Scale Test Inverter

The structure of the inverter used for testing the digital controller is shown in Figure 8. V_{DC} is 60V and the IGBTs are 800V, $12A_p$ rated BUK854-800As [8]. This low power inverter was only used for testing the controller and a larger inverter will be used for the active power filter.

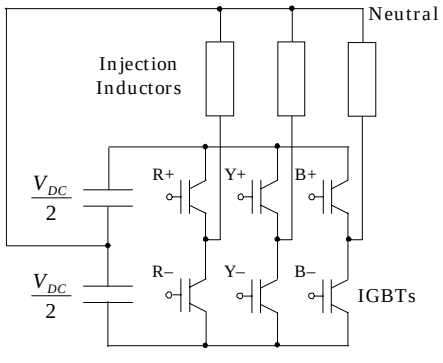


Figure 8 Small-scale test inverter.

At this stage one phase of the inverter has been implemented. The active power filter will operate with unbalanced loads and therefore each of the phases must operate independently. The neutral connection to the DC bus midpoint prevents any phase interaction [4]. A three phase inverter will be constructed now that the single phase inverter has been thoroughly tested.

4.2 Inverter Operation

Two reference waveforms were used to test the inverter. A sinusoid was initially used to verify that the inverter was operating correctly. Output frequencies from 1Hz through to 500Hz have been produced. The inverter output with a 36Hz $4.24A_{RMS}$ sinewave with $h = 0.1A$ is shown in Figure 9. The injection inductance is 9mH. The switching noise peak is at 4.65kHz and the magnitude is 2% of the fundamental.

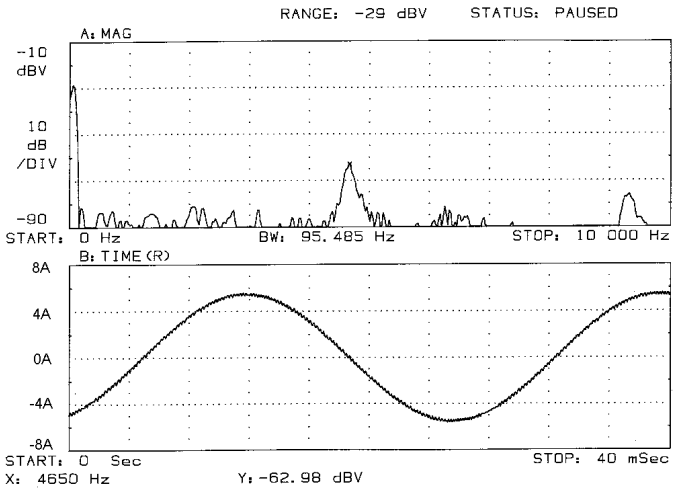


Figure 9 Sinusoidal output of the inverter in the frequency and time domains.

Figure 10 shows an expanded view of the top of the sinusoid and illustrates the ramping up and down of current through the inductor. The hysteresis band is constant with two current overshoots and noise on the signal.

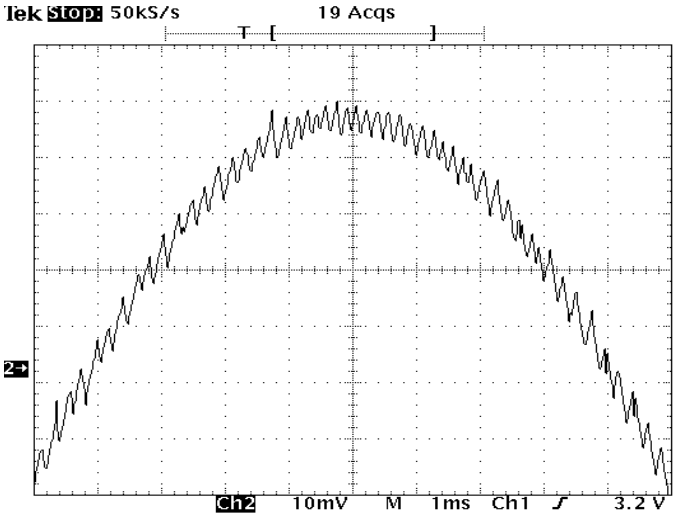


Figure 10 Expansion of the sinusoidal output showing the ramping of current. 10mV represents 0.5A.

This digital inverter controller is intended for use in an active power filter, and so a sample compensating current was generated. This current is the harmonic content of the current

drawn by a three phase bridge rectifier with a capacitive load, as illustrated in Figure 1. Figure 11 shows the spectrum and time domain waveform of this compensating current where the fundamental frequency is 50Hz and the injection inductance is 4mH. The compensating current is scaled for an overall load current of $0.71A_{RMS}$.

The slope of the current is much higher for this waveform than for the pure sinusoid and so the inverter has greater difficulty tracking the reference. Figure 12 shows the ramping of the current about the reference and illustrates the asynchronous nature of hysteresis current control. The maximum switching frequency is at 6.18kHz and is the magnitude is 0.7% of the 250Hz component of the compensating current. The switching noise is distributed over a wider band for this current, giving a lower maximum level than for the sinusoidal current. The switching frequency range associated with the sinusoidal current in Figure 9 is concentrated into a small area and this results in a peak.

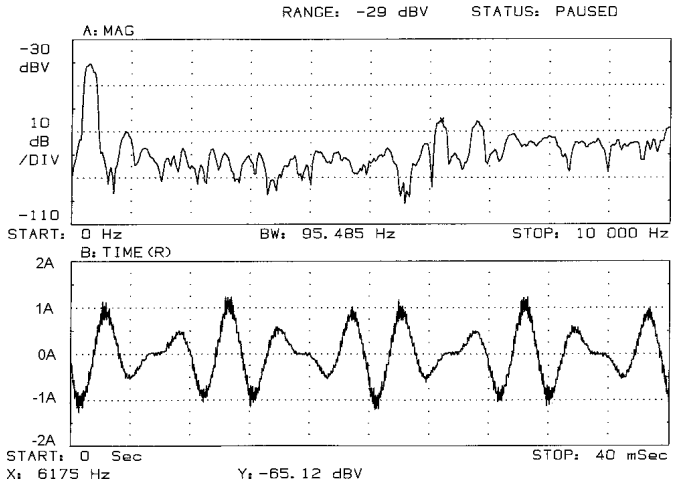


Figure 11 Compensating current output from the inverter.

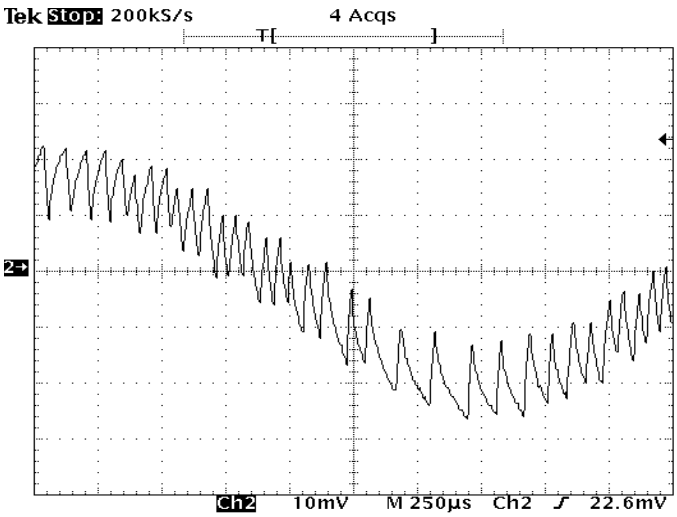


Figure 12 Close detail of the 'compensating current'. 10mV represents 0.2A.

4.3 Switching Noise

The hysteresis current controller ideally has a constant current ripple, Δi, but no defined switching period Δt [4]. The maximum switching frequency occurs in a hysteresis controlled inverter when the gradient of the reference current is near zero, as illustrated in Figure 3. To test the validity of Equations (5) and (6) the inverter was operated with a zero amplitude reference. This kept the DC current through the inductor zero. Table 1 summarises the measurements taken.

Table 1 Maximum inverter switching frequency.

h (½Δi)	Max Frequency (kHz)	
	Calculated	**Observed**
0.1	7.4	5.9
0.2	3.7	3.6
0.3	2.5	2.6
0.4	1.9	1.8
0.5	1.5	1.5
0.6	1.2	1.3

It can be seen that the calculated and observed results are very close from where h = 0.2A.

The spectra of Figure 9 and Figure 11 show the nature of the switching noise. Further tests were conducted with a single 60Hz sinusoid injected into the inductor. Table 2 shows the frequency and magnitude of the switching noise with respect to the magnitude of the 60Hz fundamental. The entries where the hysteresis limit is 10% of the peak current are highlighted.

Table 2 Relative magnitude and frequency of switching noise.

I_P (A)	h (A)					
	0.1	0.2	0.3	0.4	0.5	0.6
1.0	7.2% 7.1kHz	15.7% 3.7kHz	21.4% 2.5kHz			
2.0	2.5% 7.7kHz	6.1% 3.5kHz	10.2% 2.5kHz			
3.0	1.8% 7.8kHz	2.2% 3.7kHz	3.6% 2.4kHz			
4.0	0.8% 7.7kHz	1.8% 3.7kHz	2.3% 2.4kHz	3.3% 1.8kHz		
5.0	0.7% 7.7kHz	1.3% 3.6kHz	1.8% 2.4kHz	2.3% 1.8kHz	3.7% 1.4kHz	
6.0	0.5% 7.7kHz	0.6% 3.6kHz	1.0% 2.4kHz	1.8% 1.7kHz	2.7% 1.3kHz	3.1% 1.0kHz

The results in Table 2 show that the magnitude of the switching noise is, on average, 4% of the fundamental current when the hysteresis limit is one tenth of the reference current peak. The lowest level of switching noise was with h = 0.1A, I_P = 6.0A and was 0.5% of the fundamental and is an improvement over the 3% magnitude obtained with h = 0.6A.

The observed switching frequencies in Table 2 agree with the theoretical values from Table 1. The results in Table 2 confirm that the switching frequency is largely independent of the reference magnitude.

4.4 Noise Immunity

One benefit of digital control is that the current reference is transmitted in a serial datastream from the DSP to the inverter controller. It was predicted that this would enhance the

controller's ability to withstand electromagnetic interference (EMI).

The ability of this prototype inverter controller was tested by operating a 146.475MHz radio transmitter at a variety of distances from the controller. Even though oscilloscope waveforms showed increased noise on the voltage signal feeding to and from the Xilinx chip, there was minimal disturbance to the current waveform from the inverter.

Disturbance only occurred when the tip of the transmitting antenna was touching the Xilinx chip. The inverter failed to operate once the transmitter was stopped, and only started again when the DSP updated the reference and hysteresis limits. This suggests that a register change occurred in the Xilinx due to the high electrical fields present (about 100-200V/m). This level of EMI would seldom be found except near radio transmitters. It can be assumed that the digital inverter controller itself is not susceptible to EMI.

The one weakness in the system is the analogue to digital converter (ADC) used for digitising the current feedback (see Figure 6). The input to the ADC does show noise in the presence of EMI and so great care must be taken to ensure that this device and its associated analogue circuitry are well shielded.

4.5 Current Overshoot

The sampling frequency for the current feedback is fixed at 203kHz, and therefore some current overshoot will occur. The current swing was measured while the switching frequency tests were being performed. For this test, L = 9mH, V_{DC} = 60V and f_{Sample} = 203kHz. From Eqn. (6) the value of overshoot, Δi_{Over}, is 16mA. Table 3 summarises the level of overshoot for six values of h.

Table 3 Current overshoot from the hysteresis band.

h	Overshoot (mA)	
(A)	Predicted	Actual
0.1	16	28
0.2	16	40
0.3	16	74
0.4	16	76
0.5	16	65
0.6	16	60

Whilst the predicted maximum overshoot is independent of the hysteresis limit, h, this is not so for the experimental results. Measuring small currents is difficult and the input to the current feedback ADC has a noticeable level of noise. This will affect the inverter controller's ability to determine accurately when the current has exceeded the hysteresis band. It is expected that by dealing with larger currents the effect of noise on the analogue circuitry will be reduced.

5. Conclusion

A novel digital hysteresis current controller has been designed and implemented in a Xilinx field programmable gate array. This completely digital controller makes the switching decisions for hysteresis control and provides deadtime protection. The theoretical performance of a digital hysteresis controller has been presented. The inverter controller has been tested on a small scale inverter to verify its operation. The experimental results are close to those predicted by theory. Digital current control of an inverter appears promising and further development with larger inverters will be performed in the future.

Acknowledgments

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References

[1] H. Sasaki and T. Machida, "A New Method to Eliminate AC Harmonic Currents by Magnetic Flux Compensation", *IEEE Trans. Power Appl. Syst.*, Vol. PAS-90, No. 5, pp. 2009–2019, 1971.

[2] R.M. Duke and S.D. Round, "The Steady-State Performance of a Controlled Current Active Filter", *IEEE Trans. Power Electron.*, Vol. 8, No. 3, pp. 140–146, 1993.

[3] S.D. Round and R.M. Duke, "Real-Time Optimization of an Active Filter's Performance", *IEEE Trans. Ind. Electron.*, Vol. 41, No. 3, pp. 278–284, 1994.

[4] D.M. Brod and D.W. Novotny, "Current Control of VSI-PWM Inverters", *IEEE Trans. Ind. Applicat.*, Vol. IA-21, No. 4, pp. 562–570, 1985.

[5] Y.-H. Lee, B.-S. Suh and D.-S. Hyun, "A Novel PWM Scheme for a Three-Level Voltage Source Inverter with GTO Thyristors", *IEEE Trans. Ind. Applicat.*, Vol. 32, No. 2, pp 260–268, 1996.

[6] "The Programmable Logic Data Book", Xilinx, San Jose, California, USA, July 1996.

[7] "Third-Generation TMS320 User's Guide, SPRU031", Digital Signal Processor Products, Texas Instruments, Houston, Texas, USA, 1988.

[8] "SC13 PowerMOS Transistors including TOPFETs and IGBTs", Philips Semiconductors, Eindhoven, The Netherlands, pp 584–588, 1995.