A Novel Digital Hysteresis Current Controller for an Active Power Filter

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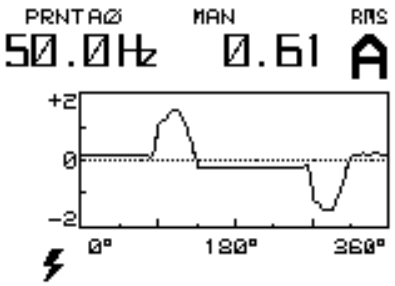
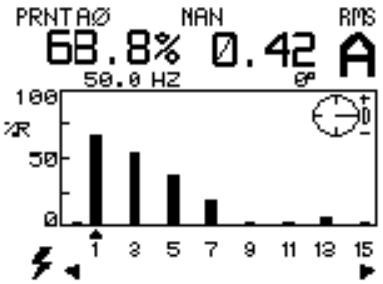
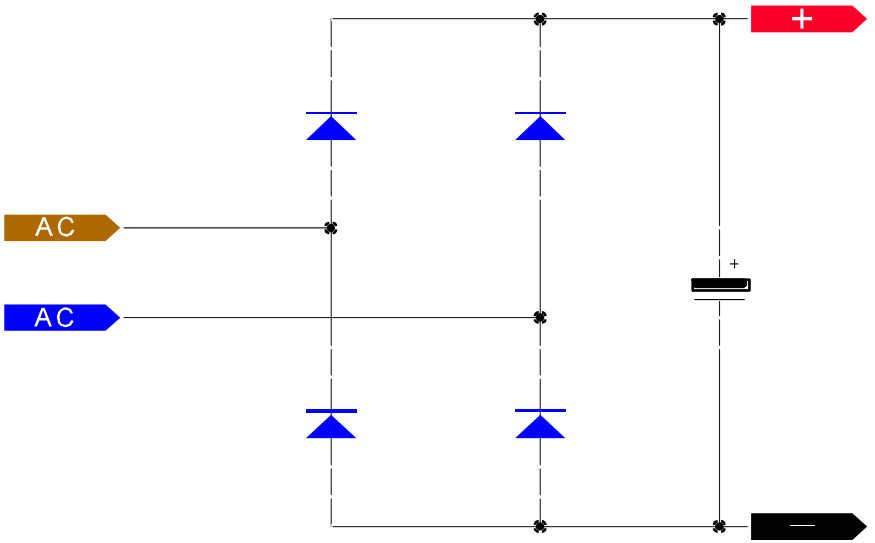
The Active Power Filter

Non-Linear Currents

➔Currents with large levels of harmonics present are drawn mainly from rectifiers with output smoothing capacitors.







The Active Power Filter

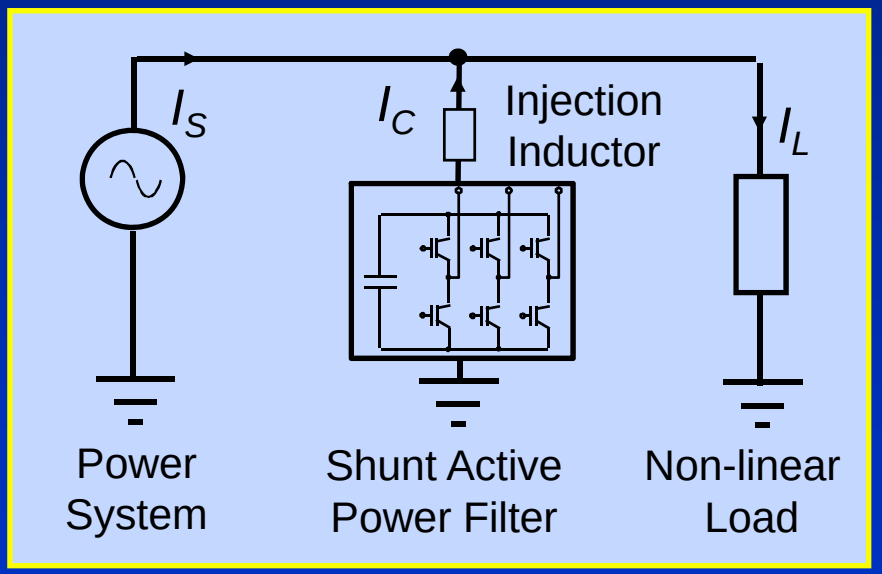
Problems Caused by Harmonics

- Overheating of electrical machinery
  - Increased RMS currents increase power loss in conductors.
- Interference to telecommunications
  - Most harmonics (7^{th} upwards) are in the audible range.
- Damage to power factor correction equipment
  - High frequency currents cause excessive heating of power factor capacitors.

The Active Power Filter

System Diagram

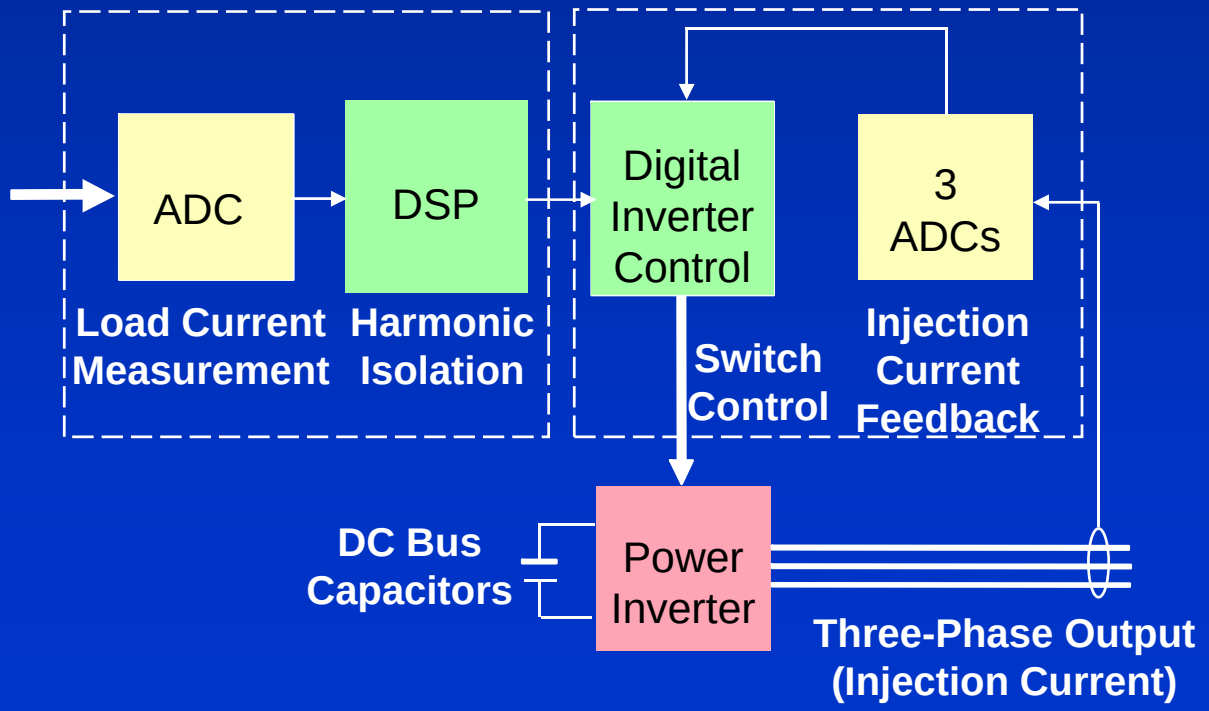
- A site draws a non-linear load current.
- This current contains harmonics.
- The Active Power Filter injects harmonic currents that cancel those drawn by the load.



The Active Power Filter

Elements of the Active Power Filter

- Harmonic Isolation
- Current Controller for the Inverter
- Three-phase power inverter

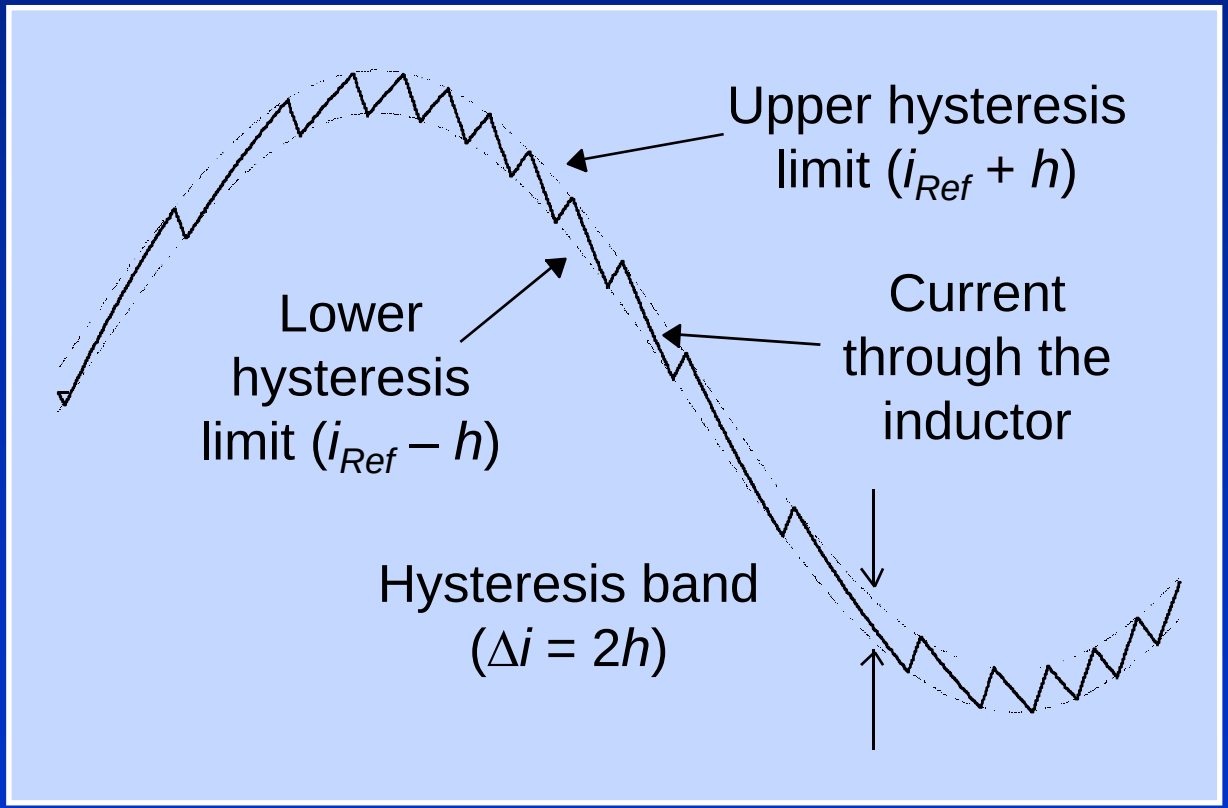


Hysteresis Current Control

Principle of Operation

The current is ramped up and down through an inductor so that it follows a reference waveform.

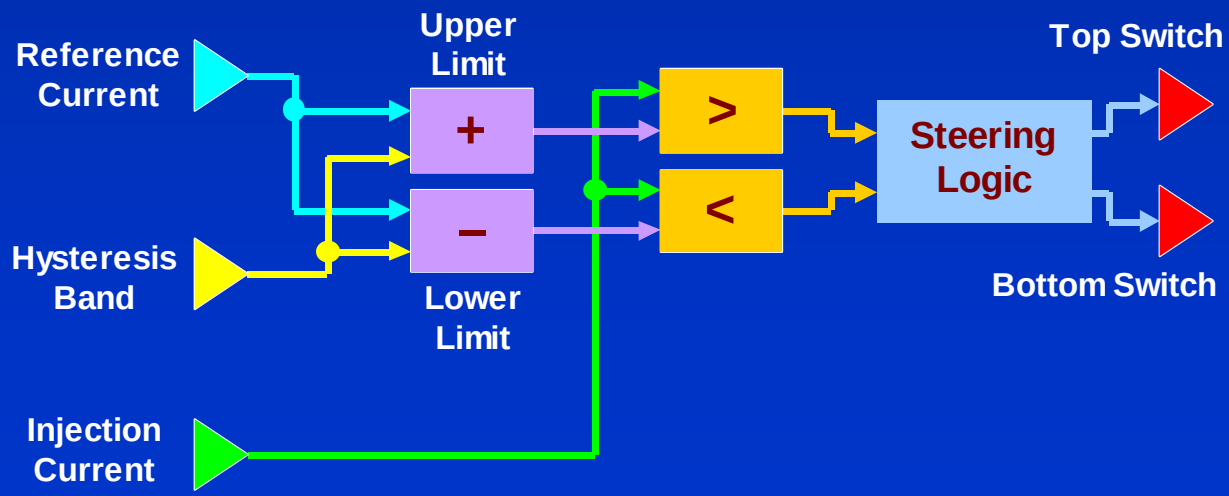
The hysteresis band is twice the hysteresis limit.



Hysteresis Current Control

Digital Inverter Control

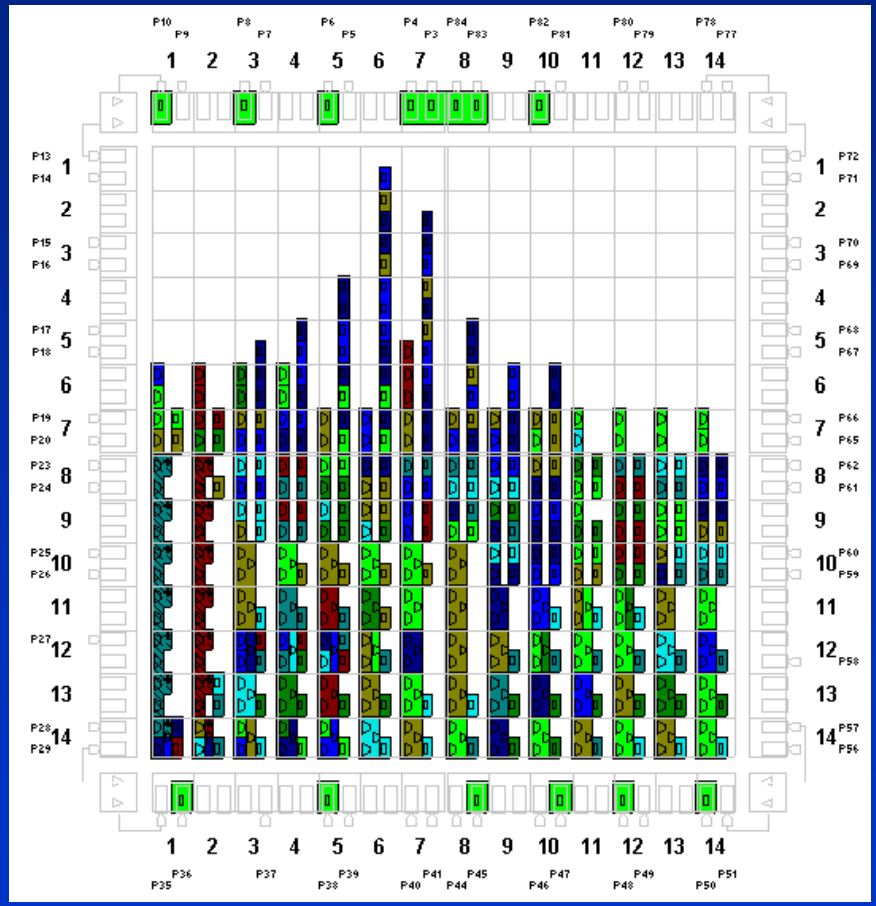
- The hysteresis limits are generated with digital adder/subtracters.
- The comparison of the injection current to the hysteresis limits is performed digitally by "2's Complement" magnitude comparators.



Hysteresis Current Control

Field Programmable Gate Arrays (FPGAs)

- Used to implement the Digital Inverter Controller.
- FPGAs contain many logic blocks that are interconnected with memory cells and can be modified without changing the circuit board.
- A single FPGA can be equivalent to thousands of logic gates.



"Floorplan" of the Xilinx 4005E FPGA with the Inverter Controller

Inverter Requirements

Injection Inductor

- The injection inductor must be chosen so:
  - The current can change fast enough to follow the high frequencies in the reference.
  - Be large enough to make the average switching frequency as low as possible to reduce losses in the inverter.
  - The maximum harmonic slope is given by:

$$\max\left(\frac{di}{dt}\right) = A2\pi f$$

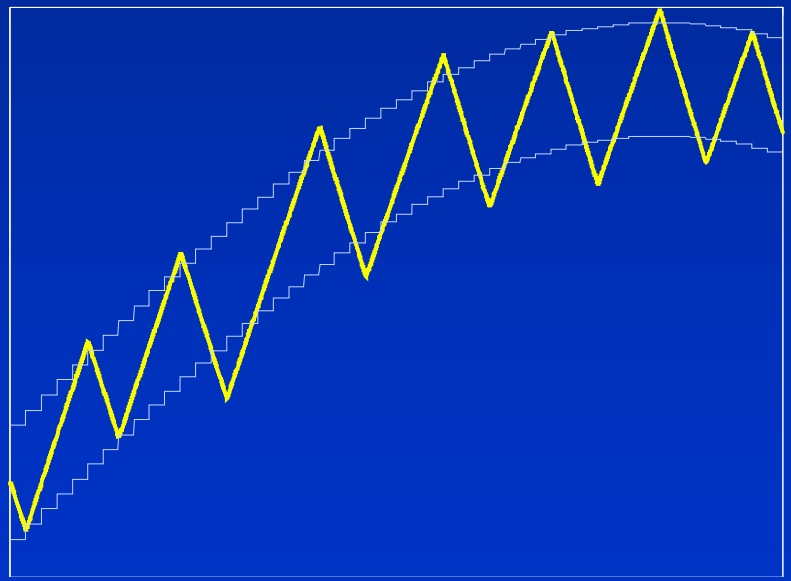
  - The current slope of the inductor is given by:

$$\frac{di}{dt} = \frac{\frac{1}{2}V_{DC} - V_{Supply}}{L}$$

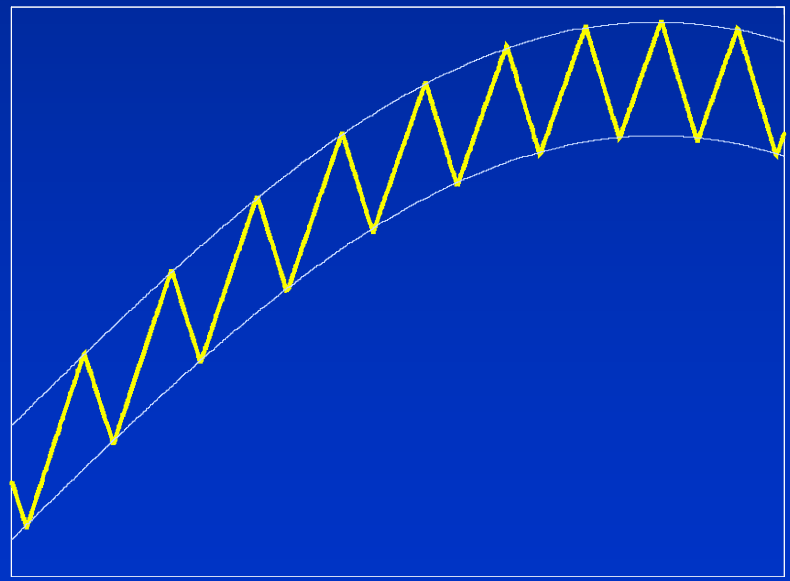
Inverter Requirements

Sampling Frequency

The digital hysteresis controller makes decisions at fixed times, rather than continuously as an analogue controller does. The more often a decision is made, the less current overshoot.



f_{sample}=10kHz

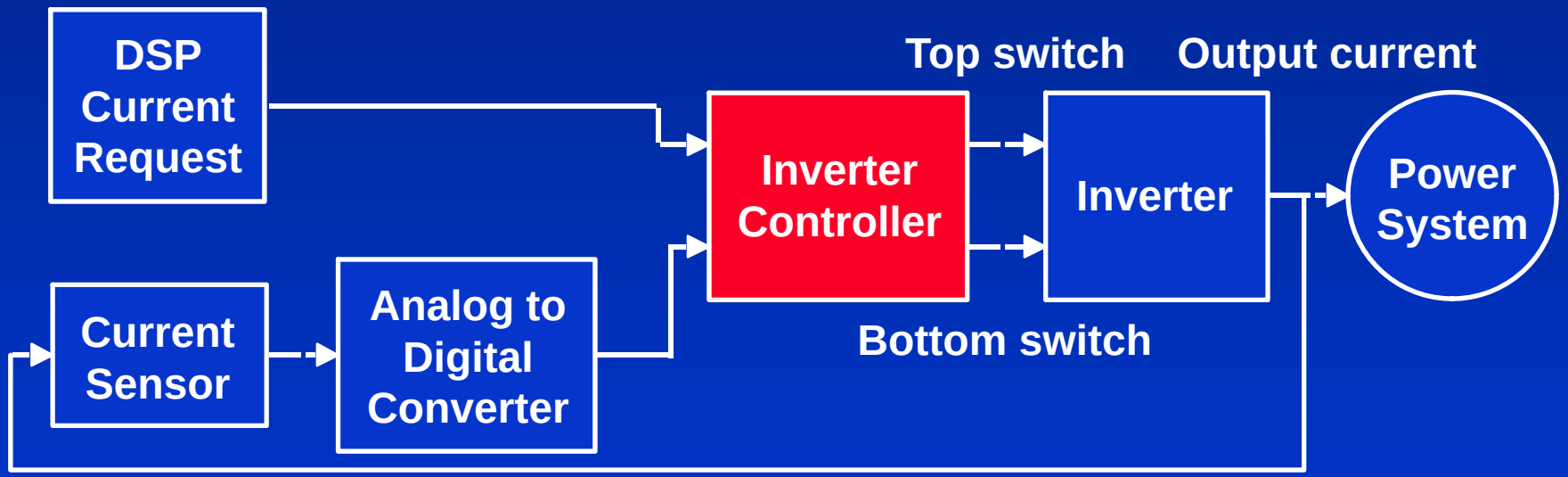


f_{sample}=200kHz

Inverter Controller Design

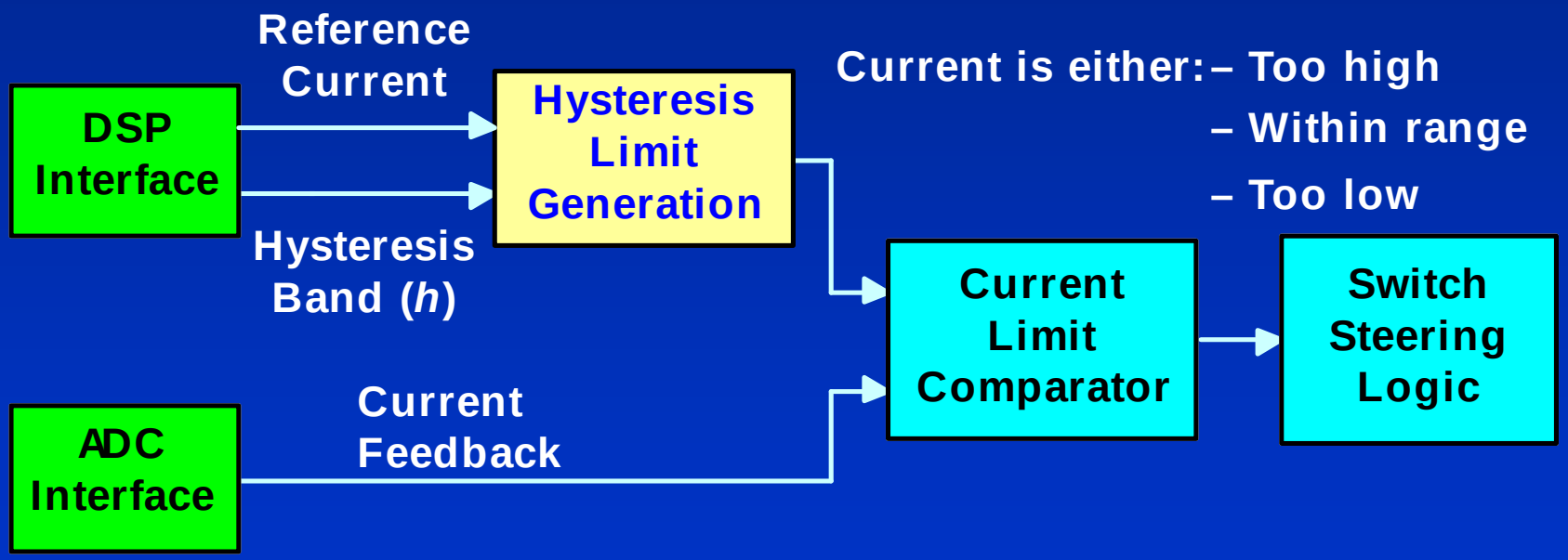
Inverter Controller System Diagram

(One of three phases)



Inverter Controller Design

Inverter Controller Block Diagram



Inverter Controller Design

Parameter Selection

- ➔ $400A_{PEAK}$ load with precision to 0.2A requires 4000 'points'. This requires 12 bit analogue to digital converters.
- ➔ Limit the current overshoot to 5A for an 800μH inductor with an $800V_{DC}$ bus,

$$\Delta i_{Over} = \frac{\frac{1}{2}V_{DC}}{L}\frac{1}{f_{Sample}}$$

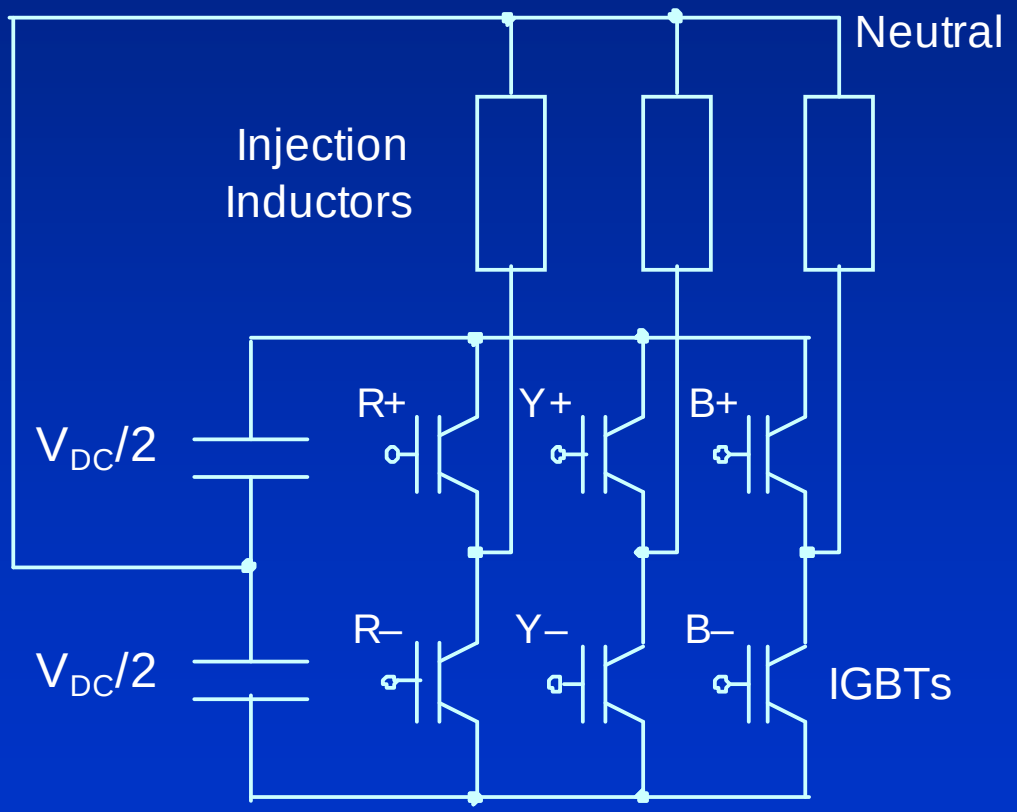
indicates that f_{sample} must exceed 100kHz. 260kHz is the used for the feedback ADCs — this is as fast as possible for the ADC used.

Experimental Results

Test Inverter

800V, $12A_{PEAK}$ IGBTs

V_{DC} is 60V



Experimental Results

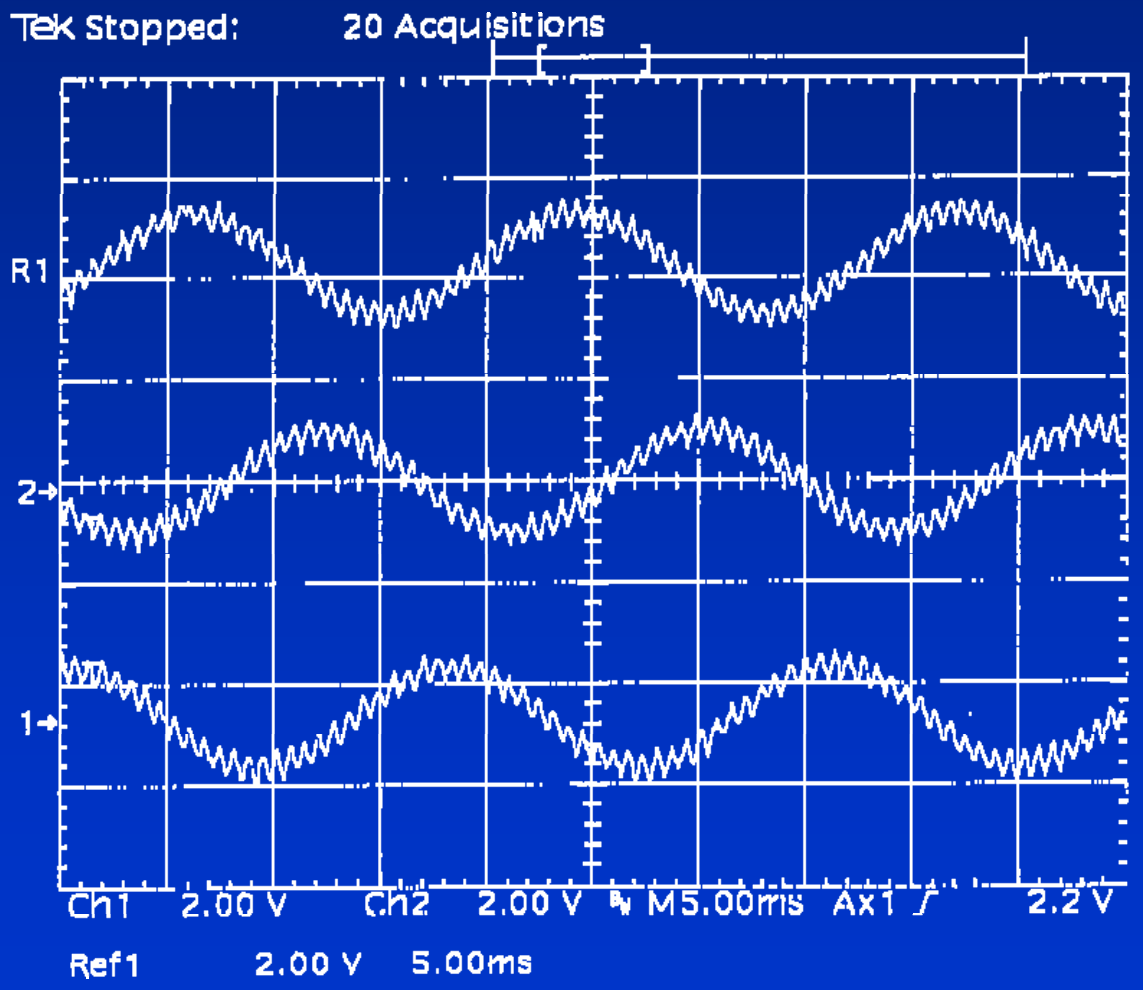
Three-Phase Output

55Hz Output

$2A_{PEAK}$

$h = 0.5A$

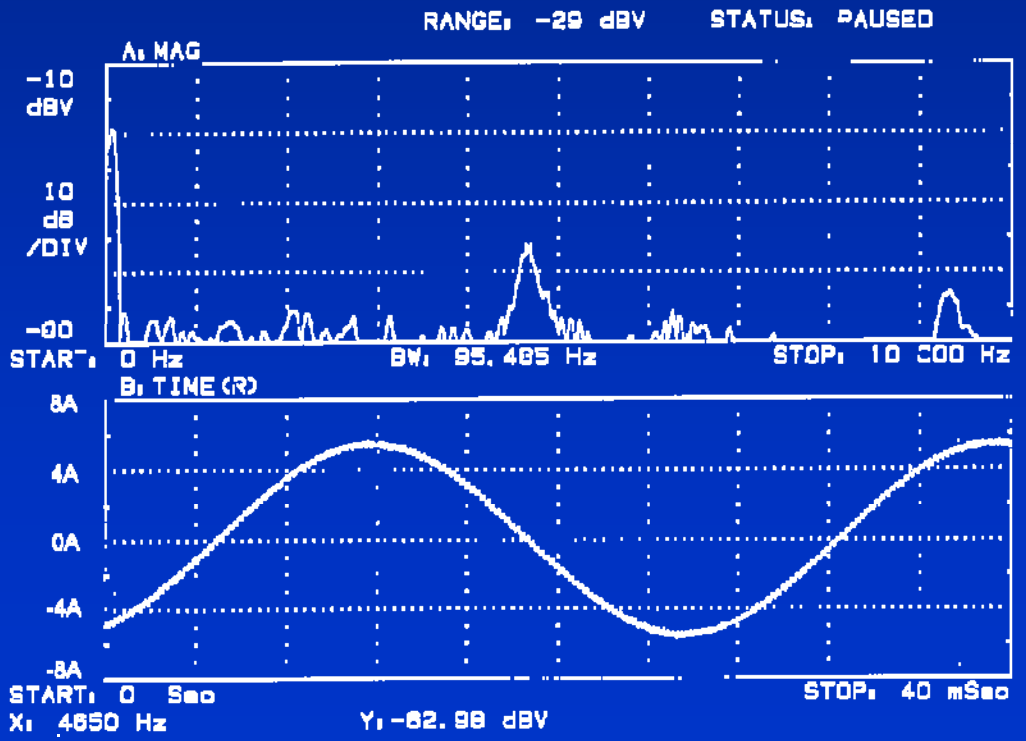
L=9mH

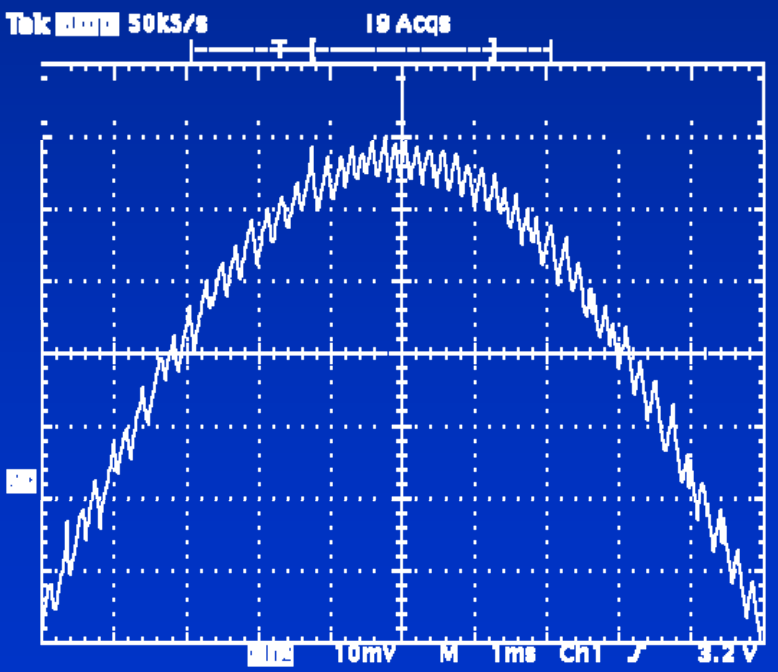


Experimental Results

Sinusoidal Outputs

The inverter output is a 36Hz 4.24A_{RMS} sinewave with ΔI=0.2A. An injection inductance of 9mH was used. The switching noise peak is at 4.65kHz and the magnitude of the noise is 2% of the fundamental.





Experimental Results

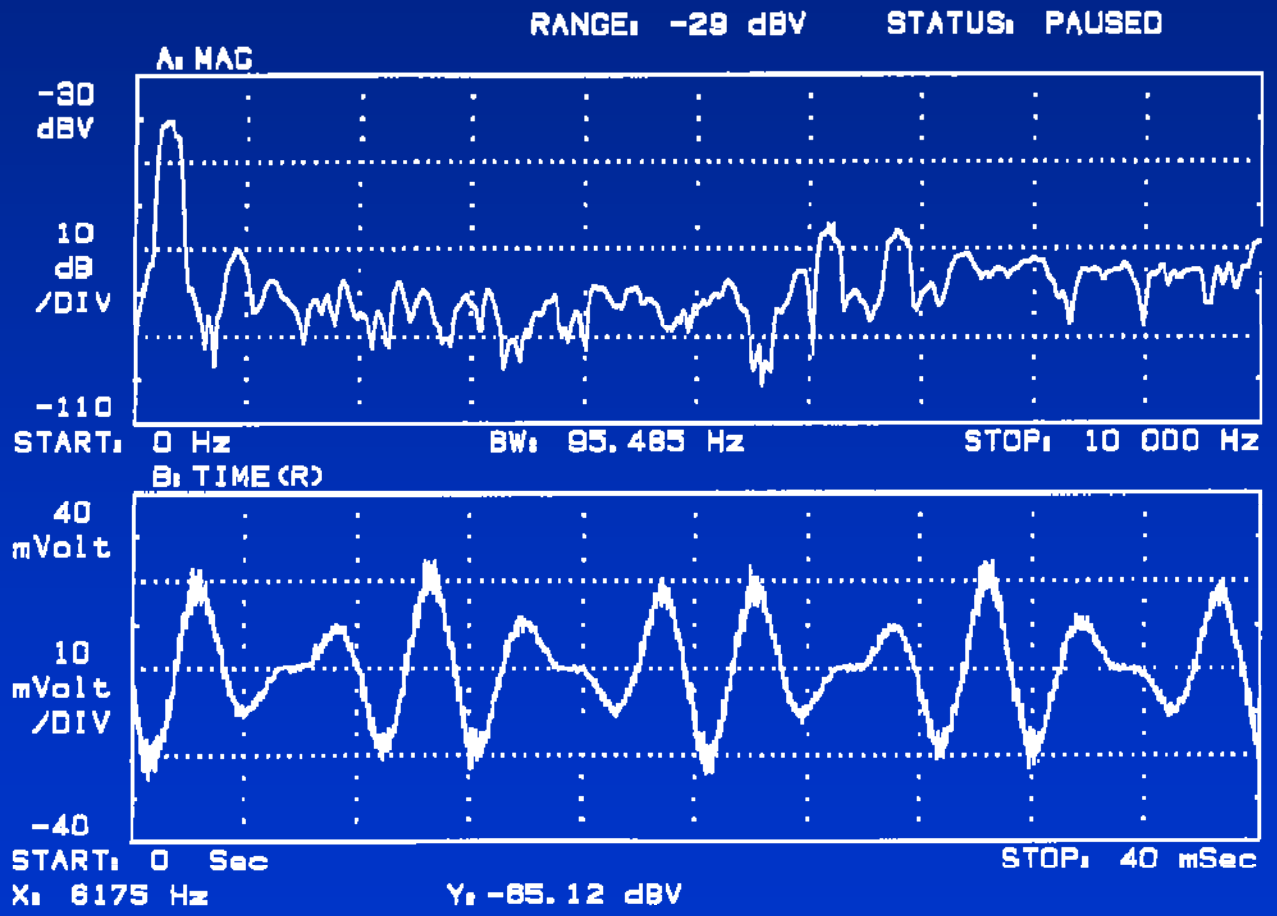
Compensation Current Output

(For three-phase bridge rectifier)

Frequency Domain

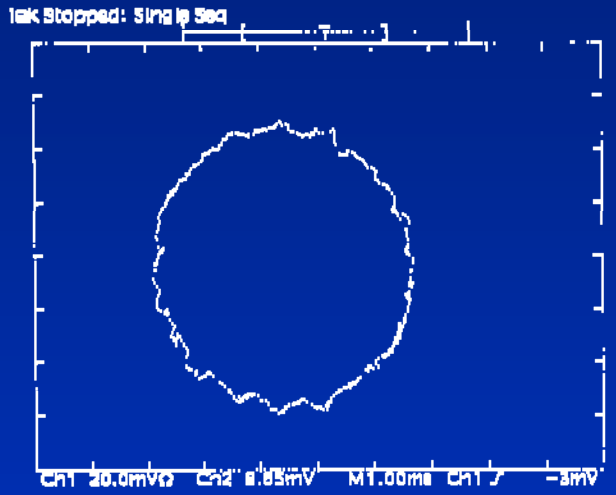
Time Domain

L=4mH

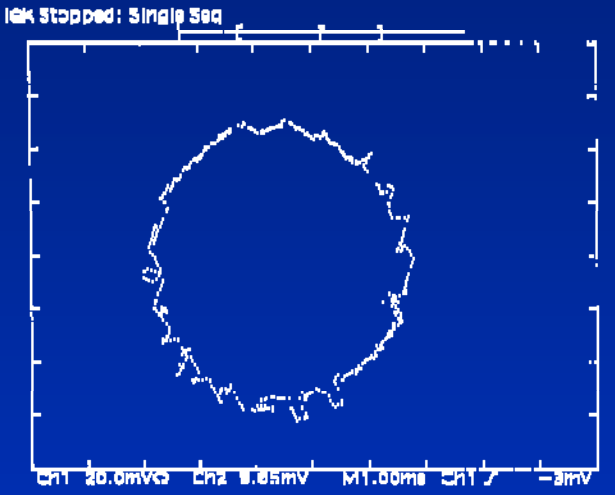


Experimental Results

Space Vector Diagrams

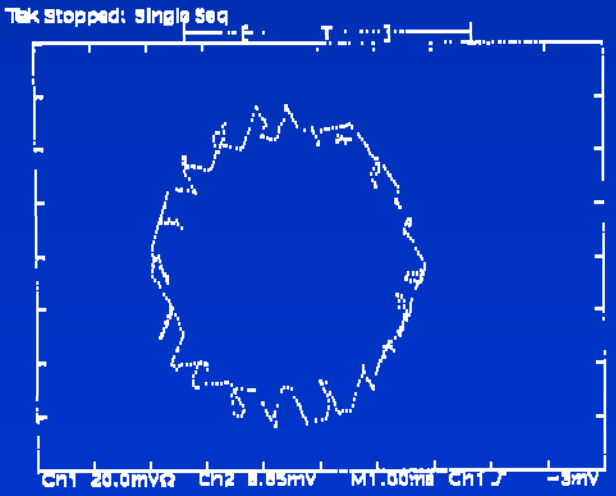


$h=0.1\text{A}$

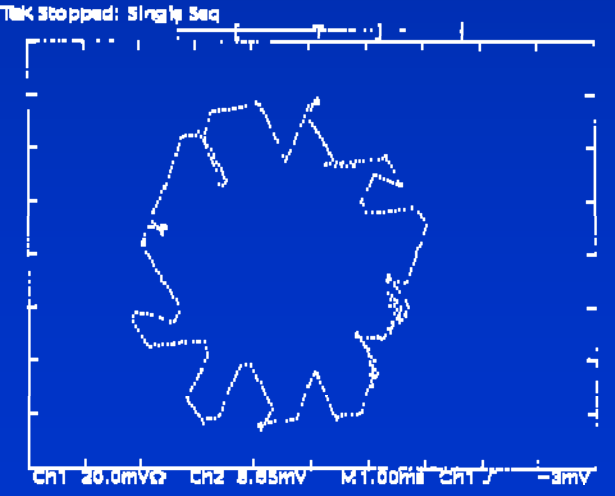


$h=0.2\text{A}$

All currents are 100Hz, 3A_{PEAK}



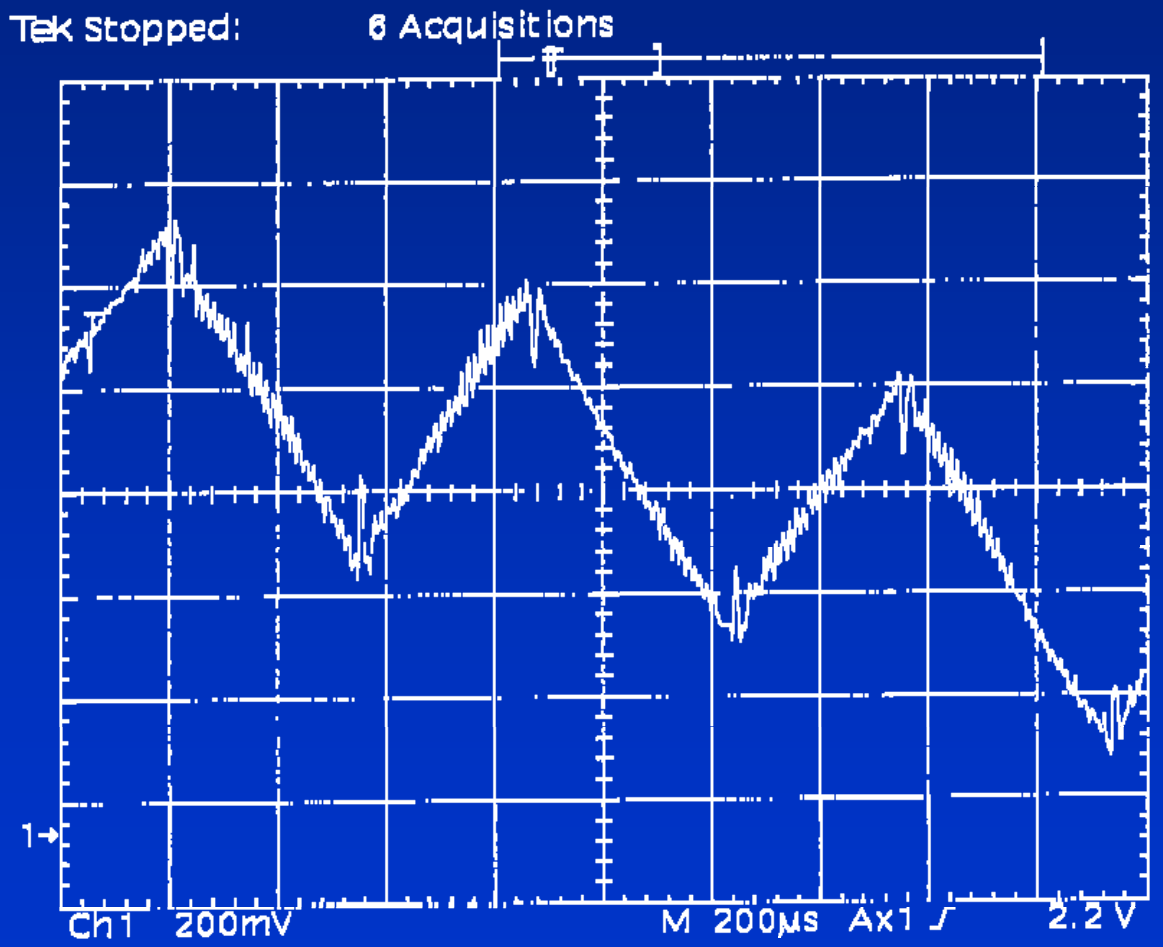
$h=0.3\text{A}$



$h=0.6\text{A}$

Experimental Results

Analogue Noise



High frequency noise is present at the inputs to the ADCs.

Any noise introduced at this point stays in the system and reduces the effective resolution of the ADCs.

Digital Hysteresis Control

Field Programmable Gate Array Implementation

- Interfaces directly to a digital signal processor
- Highly resistant to RF interference
- Very flexible control
  - The Hysteresis Band is easily changed on the fly, allowing constant frequency hysteresis control to be implemented at a later stage.
  - Very little trimming of analog components required (only the analogue to digital converters).
- Compact design that can be easily modified at a later stage without changes to board layout.

Conclusions

- A novel digital hysteresis controller has been implemented in a Xilinx FPGA and tested with a small-scale three-phase inverter.
- Current overshoots that are not present in analogue controllers result from discontinuous sampling.
- Immunity to interference is far higher due to the digital representation of the compensating current.
- An field programmable gate array implementation:
  - Is easily interfaced to digital signal processors,
  - Is compact,
  - Allows the design to be updated without changing the circuit board.

Acknowledgments

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